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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,571	10/31/2003	Kenneth Dockser	RPS920030151US1	1590

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,571	DOCKSER, KENNETH	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, and drawings filed 31 October 2003, declaration filed 31 March 2004, and information disclosure statement filed 20 May 2004.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claims 9-10, 15, and 20: The ability to store and operate on complex numbers consisting of real and imaginary portions.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 2 recites the limitation "secondary register file" in line 3. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the examiner will interpret the claim as if "secondary register" on line 2 read "secondary register file."

7. Claims 3-6 are rejected on the basis of dependencies.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 6-9, 11, and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. Patent No. 5,187,769) hereinafter referred to as Wang.

10. As per claim 1, Wang discloses a microprocessor, comprising:

a branch unit to process branch instructions and provide a fetch unit with a next instruction address; *The examiner asserts that the processor must inherently include a unit to process branches, as the specification discloses in col. 14 line 36-37. Further, the branch unit must inherently pass a next instruction address to the fetch unit if the processor is to perform jumps as disclosed.*

a load/store unit (LSU) to retrieve data from and stored data to a data memory of the microprocessor; *Col. 11 lines 11-12 disclose load/store operations in the processor. There must inherently exist a unit to perform said operations.*

an arithmetic logic unit (ALU) to performing arithmetic operations on scalar, integer data; (Fig. 3 ALUs 46, 48 and 50 and col. 14 lines 19-22)

and a vector unit (Fig. 3 ALUs 46, 48 and 50) to execute a vector instruction to perform a first operation on a first set of data operands and a second operation on a second set of operands, wherein the first and second operations differ. *The examiner asserts that the processor performs a multiply followed by an operand rotate right for the FMULR instruction listed in the col. 27 table. Both operations (multiply and rotate) operate on both sets of operands.*

11. As per claim 2, Wang discloses the microprocessor of claim 1, wherein the vector unit comprises a primary register file (Fig. 3 register file 40) and a secondary register [file] (Fig. 3 register file 42), wherein an operand field in the vector instruction specifies a register within the primary register file and a corresponding register within the secondary register file. (Col. 27 lines 22-24)

12. As per claim 3, Wang discloses the microprocessor of claim 2, wherein the vector instruction comprises fields for first, second, and third operand field (V1, V2 and V3 in col. 27 table), wherein the first, second, and third operand fields specify as many as three operands on which the first operation is to be performed and as many as three operands on which the second operation is to be performed. *The examiner asserts that the operations are performed on all three operands.*

13. As per claim 4, Wang discloses the microprocessor of claim 3, wherein the vector unit includes a 3-input primary floating point unit (Fig. 3 FPU 46) and a 3-input

secondary floating point unit (Fig. 3 FPU 48), wherein the 3-input primary floating point unit is configured to perform a floating point operation on the first set of operands and the 3-input secondary floating point unit is configured to perform a floating point operation on the second set of operands. *Col. 27 table lists instructions as "floating point operations", hence, the FPUs are configured to perform floating point operations.*

14. As per claim 6, Wang discloses the microprocessor of claim 4, where the vector unit is configured to permit either the primary register file or the secondary register file to provide the operands for the first, second, and third inputs to the primary floating point unit and the first, second, and third inputs to the secondary floating point unit. (Col. 26 lines 22-45)

15. As per claim 7, Wang discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross instruction in which the first and second operations both use at least one operand from the primary register file and at least one operand from the secondary register file. (Col. 26 lines 22-45)

16. As per claim 8, Wang discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross-replicate vector instruction in which the first and second operations are both performed using at least one common operand. *The examiner asserts that the FMULR operation performs a multiply, and then a component rotate using the same operands as the multiply.*

17. As per claim 9, Wang discloses the microprocessor of claim 2, wherein the vector unit is configured to store a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file. *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number.*

18. As per claim 11, Wang discloses a vector unit within a microprocessor, comprising:

means for receiving an instruction specifying first operand and second operands; *The examiner asserts that the vector unit must inherently contain a unit to receive instructions if it is to process said instructions.*

means for performing a first operation on a first set of data indicated by the first and second operands and a second operation on data indicated by the first and second operands, wherein the first and second operations differ. *The examiner asserts that any vector operation in the table of col. 26 constitutes the first and second operations. The first operation is carried out by FPU 46 (Fig. 3) and the second by FPU 48 (Fig. 3). The two operations differ in that they operate on different data. The first and second operands are specified per operation in the table.*

19. As per claim 13, Wang discloses the vector unit of claim 11, wherein the instruction is further characterized as specifying a third operand and wherein the first and second operations both include multiplying data specified by a pair of the operands. *The examiner asserts that the FMUL operation in col. 27 multiplies data specified by the operands and includes a third operand which functions as a destination for the multiplication in each FPU.*

20. As per claim 14, Wang discloses the vector unit of claim 11, wherein each operand indicates a primary register of a primary register file (Fig. 3 register file 40) and a corresponding secondary register of a secondary register file (Fig. 3 register file 42). *The examiner asserts the primary and secondary registers are selected by the value held in the operands and are selected from their respective register files.*

21. As per claim 15, Wang discloses the vector unit of claim 11, wherein the primary register is configured to store a real portion of a complex number and the corresponding secondary register is configured to store an imaginary portion of the complex number. *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number.*

22. As per claim 16, Wang discloses a microprocessor including:

an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of operand fields and an operation code (opcode); *The examiner asserts that the table of col. 27 discloses operations, each with a set of operand fields. Each instruction must inherently include an opcode, so as to identify which instruction is to be performed by the processor.*

wherein the execution unit is configured to interpret the opcode to perform a first operation on a first set of data indicated by the set of operand fields and to perform a second operation on a second set of data indicated by the set of operand fields, wherein the set of operand fields indicate different sets of data with respect to the first and second operations and further wherein the first and second operations are mathematically different. *The examiner asserts that the processor performs a multiply followed by an operand rotate right for the FMULR instruction listed in the col. 27 table. Both operations (multiply and rotate) operate on both sets of operand fields. The operand fields specify operands in both register files 40 and 42, constituting different sets of data.*

23. As per claim 17, Wang discloses the microprocessor of claim 16, further comprising a vector register file for use in executing the asymmetric instruction, wherein the register file includes a primary register file (Fig. 3 register file 40) and a secondary register file (Fig. 3 register file 42), and wherein each operand in the set of operand

fields indicates a register in the primary register and a corresponding register in the secondary register file. (Col. 27 lines 22-24)

24. As per claim 18, Wang discloses the microprocessor of claim 16, wherein the instruction includes indicates first, second, and third operand fields (V1, V2 and V3 in col. 27 table) indicating first and second sets of data on which the first and second operations are performed. *The examiner asserts that the operations are performed on all three operands.*

25. As per claim 19, Wang discloses the microprocessor of claim 16, wherein each operand indicates a primary register in a primary register file and a corresponding secondary register in a secondary register file. (Col. 27 lines 22-24)

26. As per claim 20, Wang discloses the microprocessor of claim 19, wherein the primary register file is configured to store a real portion of a complex number and wherein the secondary register file is configured to store an imaginary portion of a complex number. *The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number.*

27. Claims 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (U.S. Patent No. 6,438,680) hereinafter referred to as Yamada.

28. As per claim 11, Yamada discloses a vector unit within a microprocessor, comprising:

means for receiving an instruction specifying first operand and second operands; *The examiner asserts that the vector unit must inherently contain a unit to receive instructions if it is to process said instructions. Further, multiple operations are issued as a part of the instruction pictured in Fig. 2A. The first operand listed for each operation constitutes the "first operands" and the second listed for each operation constitute "second operands."*

means for performing a first operation on a first set of data indicated by the first and second operands and a second operation on data indicated by the first and second operands, wherein the first and second operations differ. *The examiner asserts that any two different operations chosen from the list beginning in col. 9 constitute differing operations.*

29. As per claim 12, Yamada discloses the vector unit of claim 11, wherein the first operation is selected from an addition operation and an addition and negate operation and wherein the second operation is selected from a subtract operation and a subtract and negate operation. *The examiner asserts that the first operation in the instruction word is selectable to be "add" and the second to be "subtract" (instruction set beginning in col. 9).*

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Matsuo et al. (U.S. Patent No. 5,901,301) hereinafter referred to as Matsuo.

32. As per claim 5, Wang discloses the microprocessor of claim 4, but fails to disclose wherein the 3-input primary floating point unit is configured to multiply first and third operands and further configured to add the second operand to or subtract the second operand from the resulting product.

33. Matsuo discloses wherein a 3-input primary floating point unit is configured to multiply first and third operands and further configured to add the second operand to or subtract the second operand from the resulting product. (Col. 27 lines 47-52)

34. Matsuo discloses his invention to promote "high-speed digital signal processing" by taking advantage of "processing frequently used in signal processing such as a multiply-add operation at high speeds." (Matsuo col. 1 lines 13-16) Wang discloses "DSPs were developed to exploit the successive multiply/accumulate nature of signal processing." (Wang col. 3 lines 24-26) Matsuo's desired outcome of higher processing speeds through optimizing common instructions coincides with that of Wang.

35. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Matsuo's method of adding a third operand to the product of first and second operands in Wang's invention for the benefit of higher speed processing.

36. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Golliver et al. (U.S. Publication No. US 2002/0004809) hereinafter referred to as Golliver.

37. As per claim 10, Wang discloses the microprocessor of claim 9, but fails to disclose wherein the vector unit is configured to perform a complex operation in which the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

38. Golliver discloses a vector unit configured to perform a complex operation in which the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation (AiBi in Fig. 3A) and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (AiBr in Fig. 3A).

39. Golliver discloses "a data manipulation instruction for enhancing value and efficiency of performing complex arithmetic instructions." (Paragraph 2) Golliver's desired outcome coincides with that of Wang: increased efficiency of processing.

40. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Gollivers method of complex number arithmetic in Wang's processor for the benefit of increased processing efficiency.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Seshan (U.S. Patent No. 6,061,787) discloses a processor consisting of multiple parallel register files.

Tromp et al. (U.S. Publication No. US 2005/0283592) disclose a system executing two operations based on a single instruction.

Gochman et al. (U.S. Patent No. 6,920,546) disclose a system with multiple operations in an instruction word sharing common operands.

42. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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